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# IPC-2141

## Controlled Impedance Circuit Boards and High Speed Logic Design

Amendment 1

**IPC-2141**

A standard developed by IPC

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Amendment 1  
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2215 Sanders Road, Northbrook, IL 60062-6135  
Tel. 847.509.9700 Fax 847.509.9798  
[www.ipc.org](http://www.ipc.org)

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### **Standards Should:**

- Show relationship to DFM & DFE
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

### **Standards Should Not:**

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

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# Controlled Impedance Circuit Boards for High Speed Logic Design Amendment 1

## 2.0 References – change paragraph title to **Applicable Documents**

Remove references to **IPC-L-108**, **IPC-L-109** and **IPC-L-115**.

Insert reference to **IPC-4101** Specification for Base Materials for Rigid and Multilayer Printed Boards.

**3.3.1 Board Design** – Second paragraph, second sentence, change to: “... on the same wiring layer as orthogonal routing may allow ...”

Fourth paragraph, add bullet: “ • minimize crosstalk”

**3.4 Performance Requirements** – On last line, change “AC” to “analog”

**Table 2 Typical data for some logic families** – Change heading “**Wavelength**” to only be over “**In free space**” and “**In FR-4**” columns. Insert “**Critical Length**” heading over “**½ Rise FR-4**” column.

**Table 3 Propagation time in various materials** – Last column change heading “**VELOCITY**” to “**PROPAGATION DELAY**”

In legend, change BT to Bismaleimide.

**3.4.12.3 Ring Back** – First sentence, change to: “... or exceeding the logic threshold, then recrossing the ...”

**4.0 Design of Controlled Impedance Circuits** – Third paragraph, change second sentence to: “However, this may also result ...”

Fourth paragraph, change third sentence to: “... design of IC’s and can affect how many receivers may be ...”

**4.2.2 Embedded Microstrip, Figure 4d** – formula for  $C_0$  is missing a “)”, change to:

$$C_0 = \frac{[1/(H+T)/\ln(1-0.6897(\epsilon_r' + 1.41))]}{\sqrt{\epsilon_r'}} \text{ in pF/in}$$

Change definition of  $\epsilon_r'$  to read “is the effective relative permittivity...”

Add definition:  $\epsilon_r$  is the relative permittivity

**4.2.4 Dual (Asymmetric) Stripline, Figure 4f** – formula for  $C_0$  is missing a “)”, change to:

$$C_0 = \frac{2.82\epsilon_r}{\ln\left[2H - \frac{T}{(0.268W + 0.335T)}\right]} \text{ in pF/in}$$

**4.3 Balanced Line Configuration** – Fourth paragraph, last sentence, change end to read: “but CMOS and TTL logic do not, except line drivers.”

**4.7 Controlled Impedance Coupon Design Rules** – Change the first sentence of item b) to read: “Have a continuous power/ground over and under the conductor.”

Change item m) to read: “ ... impedance conductor to the grid shall be 2.5 mm minimum and the pattern length ...”

Omit the word “etch” from item o)

**9.2.1.3 Rise Time & Bandwidth Requirement** – First paragraph, change last sentence to read “System rise time ( $t_r$ ) in nanoseconds and bandwidth...”

Insert Figure 8a:

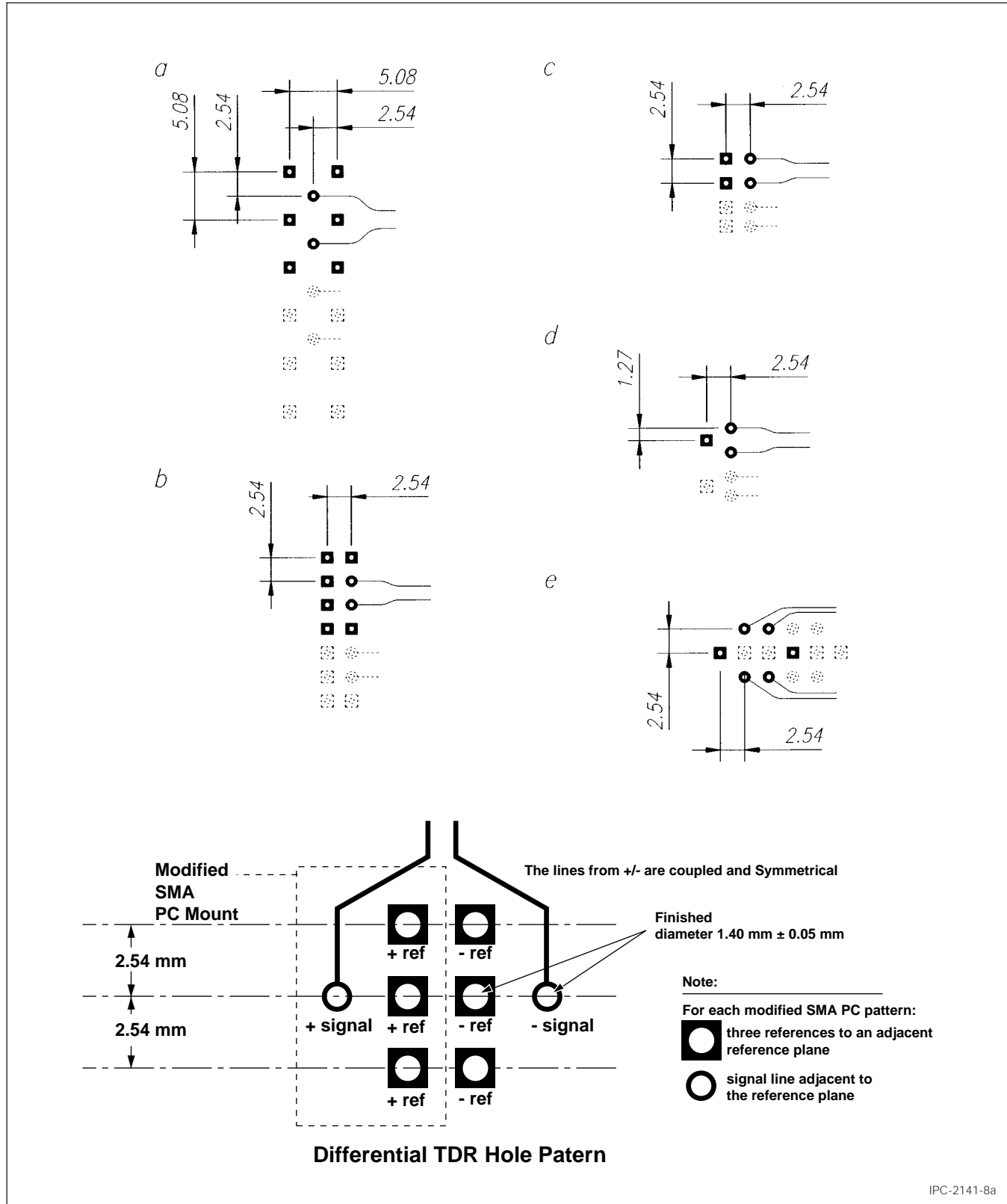


Figure 8a Typical Differential Impedance Connection Patterns

Replace Figure 10 as follows:

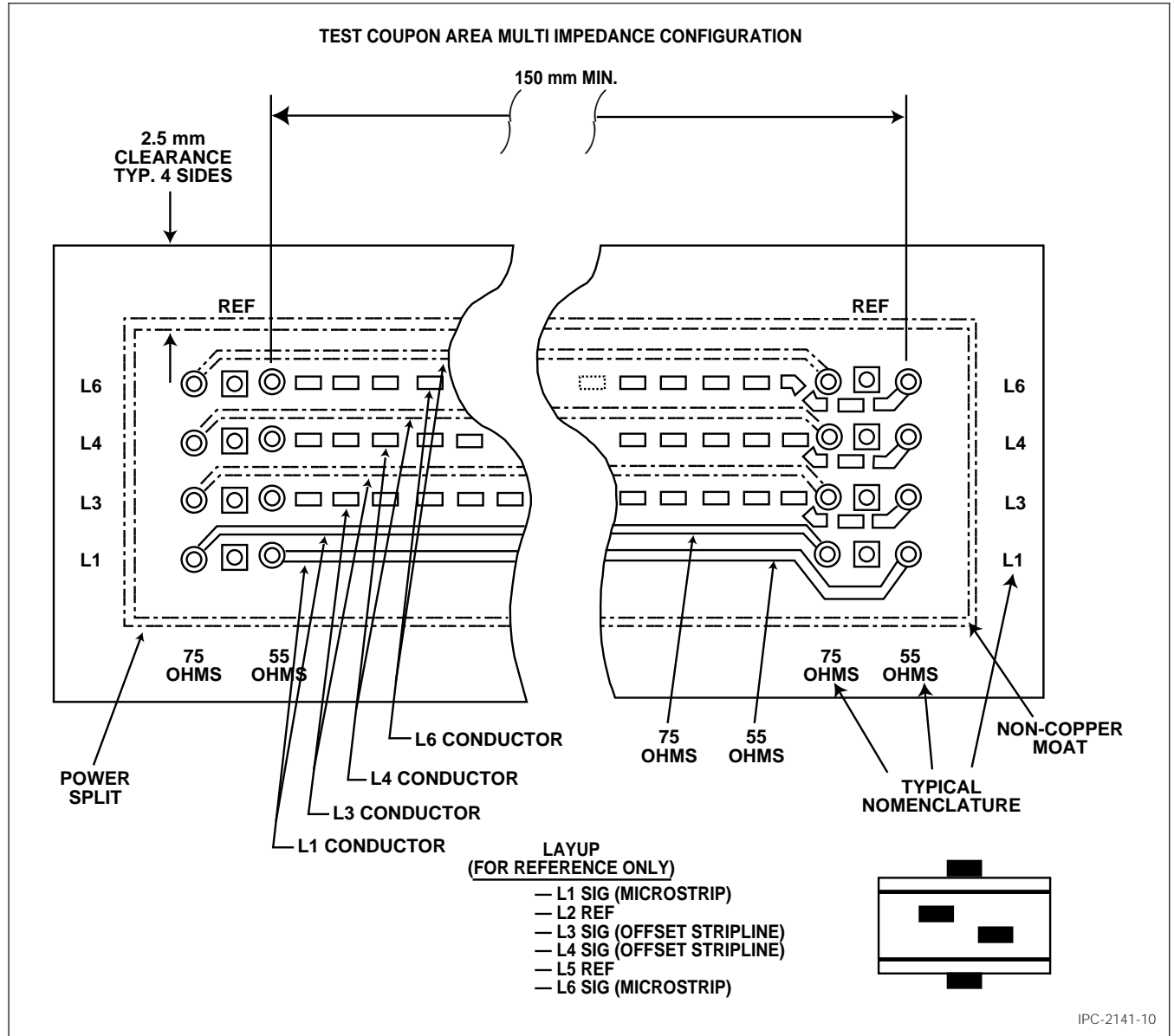
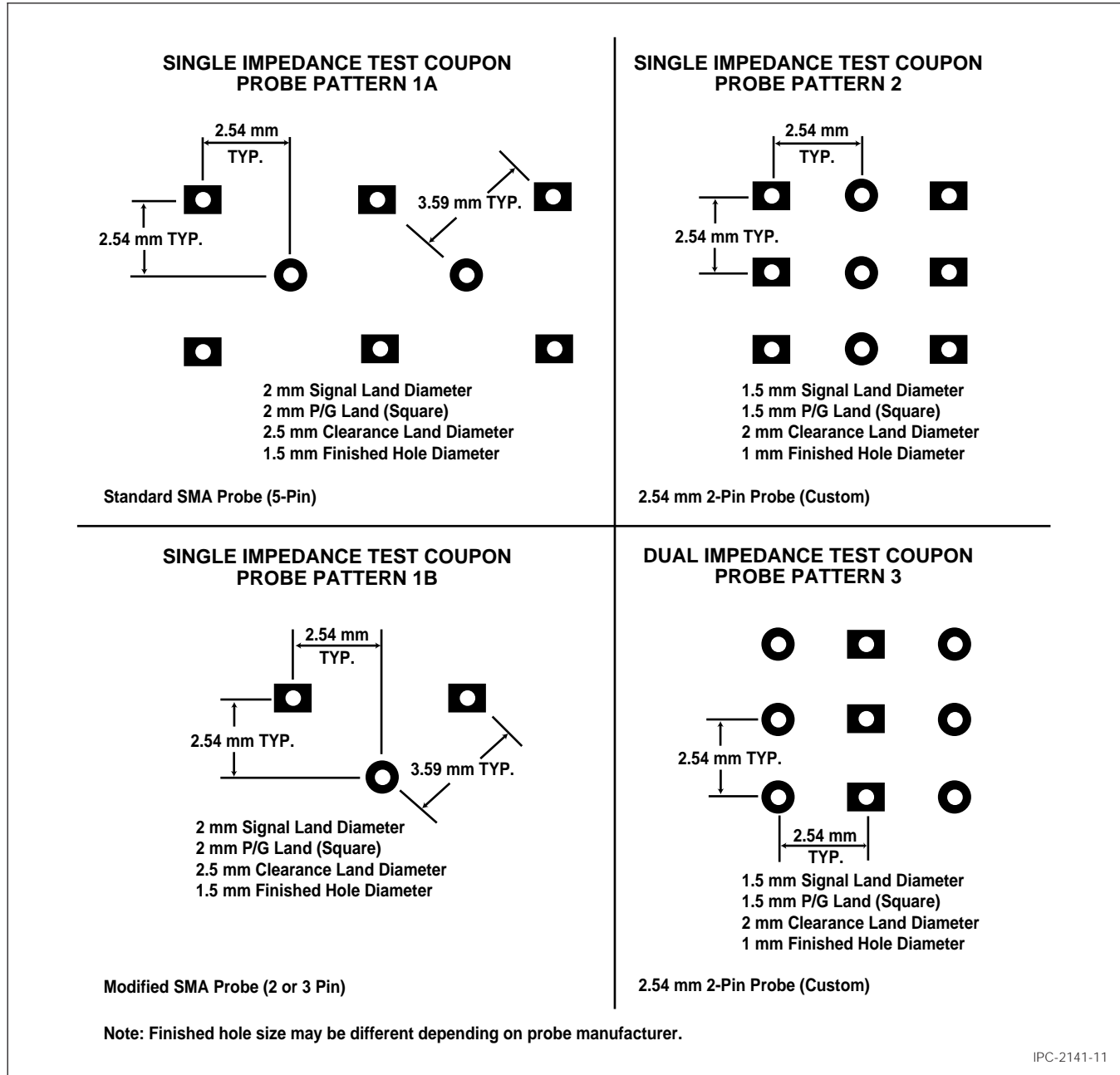


Figure 10 Impedance Control Test Coupon

Replace Figure 11 as follows:



IPC-2141-11

Figure 11 Impedance Control Test Coupon

Replace Figure 14 as follows:

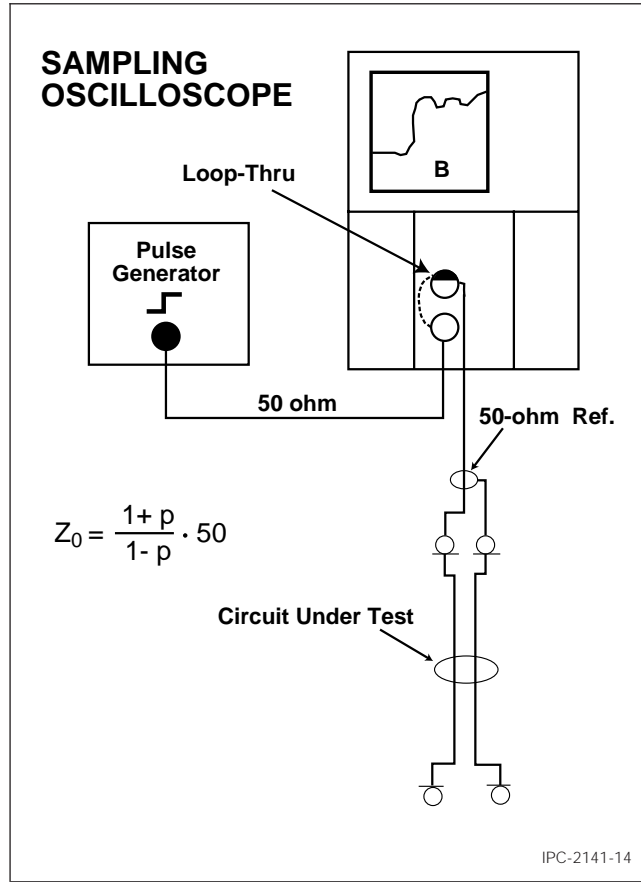


Figure 14 Typical TDR Test Set Up, Unbalanced Line

Replace Figure 16 as follows:

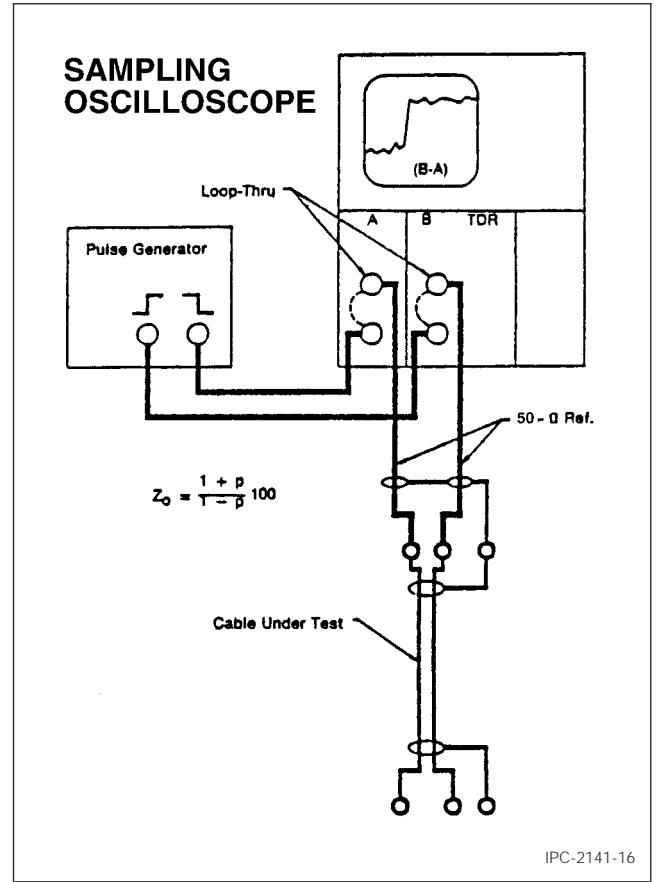


Figure 16 Typical TDR Test Set Up, Balanced Line

